Implementation of Switching Circuit Models as Vector Space Transformations

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ABSTRACT

A **transfer function** is a mathematical function relating the response of a system to its stimulus. It is a model widely used in many areas of engineering including system theory and signal analysis.

Algebraic Decision Diagrams (ADD) are canonical representations of Boolean functions. We implement a framework to build transfer function models of digital switching functions using ADDs and we demonstrate their application to simulation and justification. A prototype is used to generate experimental results and to illustrate the viability of the linear algebraic model as a basis for **EDA applications**.

The **Algebraic Normal Form** of a **cryptographic function** is of general interest since this form allows for the computation of the **algebraic degree** of the function. We present a technique whereby a degree can be extracted through a traversal of a netlist with complexity O(n).

PROBLEM STATEMENT

- Conventional switching circuits are modeled using binary-valued Boolean algebra.
- Representations used in traditional switching theory are exponentially complex.
- Justification, simulation, and SAT engines used in modern EDA tools have high computational complexity.
- Computation of the ANF of cryptographic functions is a computationally expensive process.

EXPERIMENTAL TECHNIQUES

Verilog netlist

↓

Parsing and partitioning

↓

Variable reordering

↓

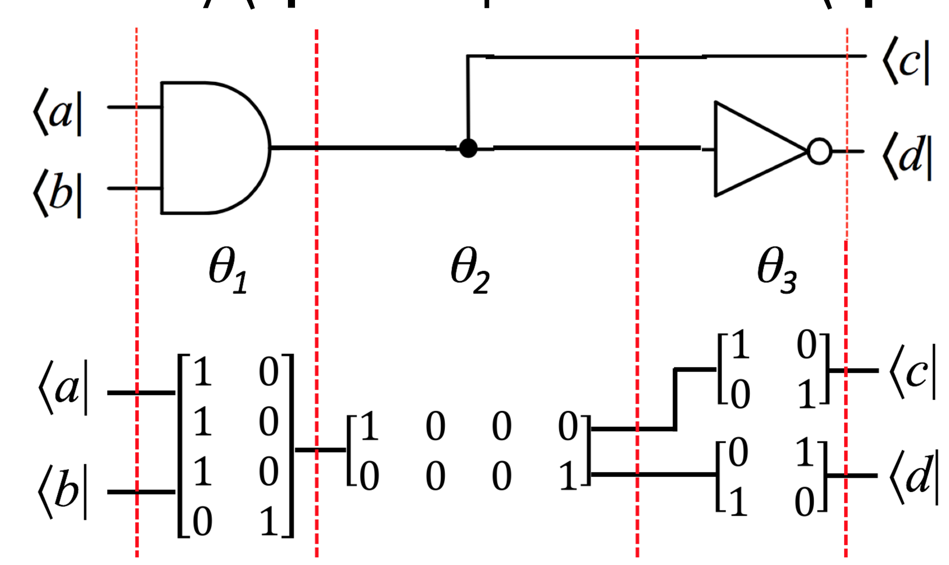
Monolithic Transfer Function or **Array Transfer Function**

↓

Output response

PROTOTYPE SIMULATOR

The first prototype uses sparse **matrices**. The output response of a logic network stimulated by an input **⟨x|** and modeled by a transfer matrix **T** is denoted by **⟨f|**. The equation used is **⟨f| = ⟨x| . T**

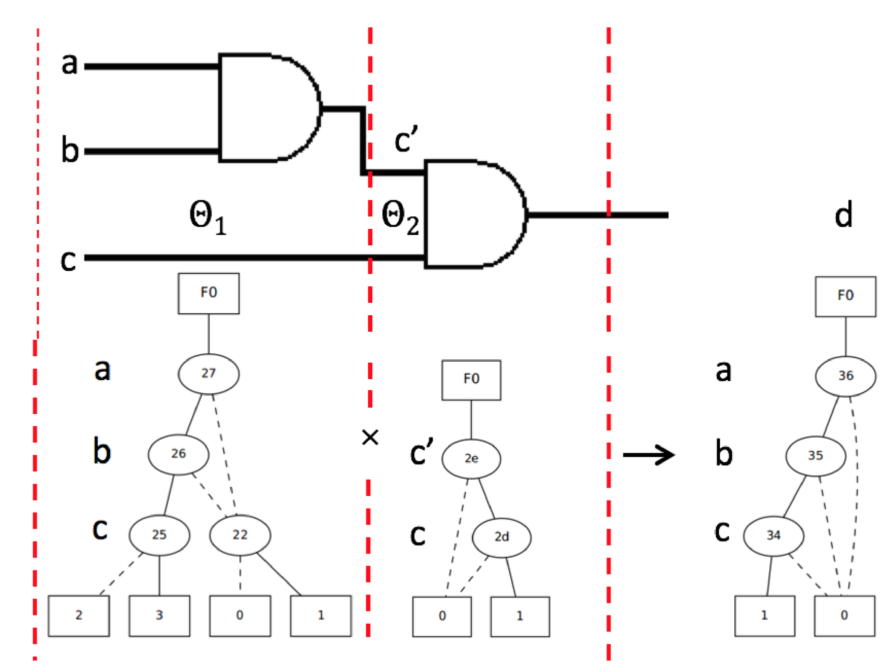


$$T_{\theta_1} \cdot T_{\theta_2} \cdot T_{\theta_3} = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \times \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix}$$

The second prototype uses **Algebraic Decision Diagrams**. We model the transfer function using directed acyclic graphs.

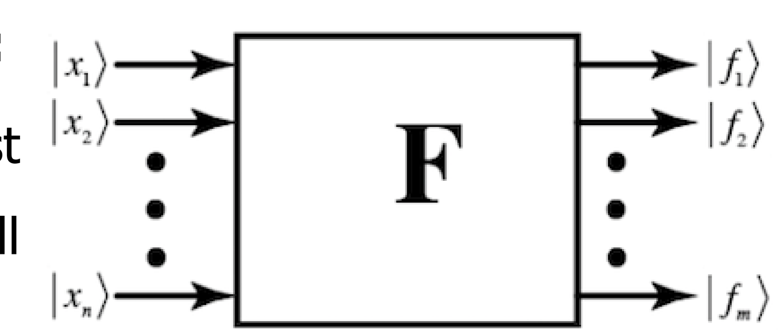
The multiplication of two decision diagrams is:

A row transformation of the multiplier diagram by the multiplicand diagram



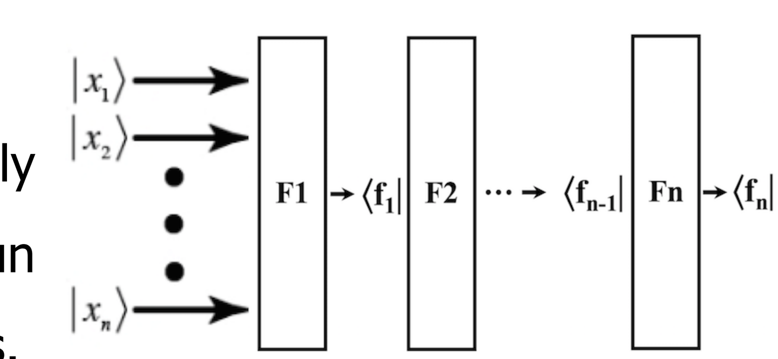
The monolithic transfer function:

Combine all partitions of the netlist into a single block. Build the overall circuit as **one ADD.**



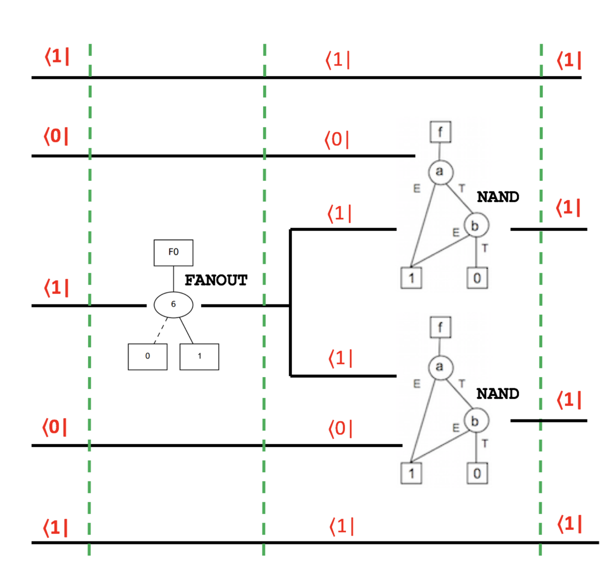
The array transfer function:

Perform the simulation incrementally starting from the primary inputs. Run multiple vector-matrix multiplications.

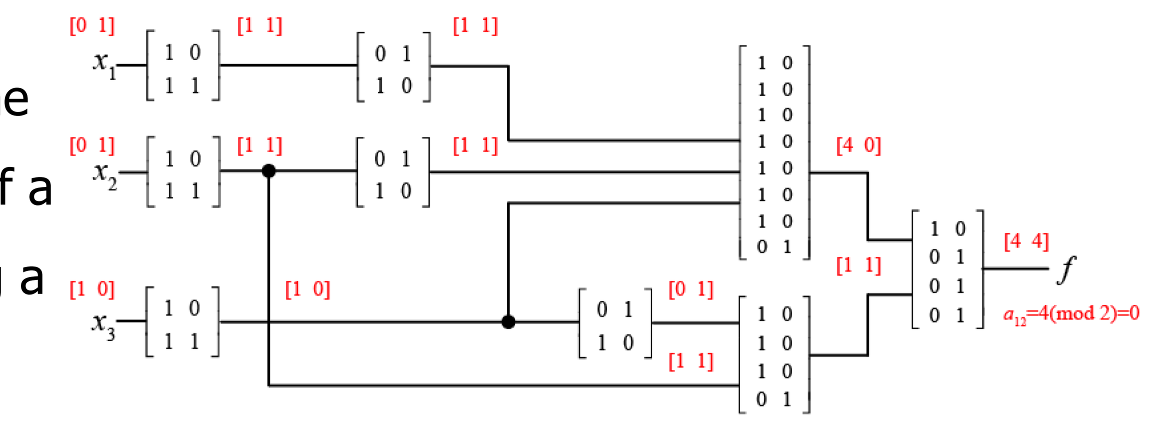


The distributed factored form:

Replace each logic gate by its corresponding ADD. Traverse the circuit by simulating each gate one at a



We can also obtain the **Algebraic Degree** of a function by traversing a structural netlist.



RESULTS

Benchmark	Inputs Outputs	# of partitions	Partitioning Time (ms)	ADD (ms) Computation	Simulation Time (ms)
con1.v	7/2	14	2.14	175.67	0.01
radd.v	8/5	28	4.91	296.04	0.03
rd73.v	7/3	24	5.56	76.96	0.01
mux.v	21/1	26	7.61	43.47	0.01
c432.v	36/7	57	240.60	945.89	0.08
c499.v	41/32	16	246.50	850.11	0.09
c1355.v	41/32	16	291.14	928.19	0.12
c880.v	60/26	67	1412.62	6580.10	0.21
c5315.v	178/123	80	3150.11	7783.62	0.37
c2670.v	233/140	99	6521.43	8195.09	0.58

CONCLUSION

- We presented a new **topology** to represent the **transfer functions** of switching circuits.
- The transfer function model can be used to performed **simulation** and **justification** in linear time.
- A new algorithm for **tensor multiplication** is formulated as an operation over **Algebraic Decision Diagram**. The algorithm enables our simulation methods to have a competitive **runtime** and **memory usage**.
- We developed a method to extract the **algebraic degree** of switching functions.
- Future research can reuse our method in **applications in EDA tools**.

PUBLICATIONS

Mitchell Thornton. Simulation and implication using a transfer function model for switching logic. **IEEE Transactions on Computers**, February 2015.

D. Houngninou and M. A. Thornton. Implementation of switching circuit models as transfer functions. 2016 **IEEE International Symposium on Circuits and Systems (ISCAS)**

D. Houngninou and M. A. Thornton. Simulation of Switching Circuits using Transfer Functions. 2017 **IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)**

D. Houngninou and M. A. Thornton. Efficient Computation of Switching Function Degree and Algebraic Normal Form. **IEEE Transactions on Computers** (Under review)