EE454 Hardware project 1

Project 1 Report

Title: Pulse Monitor

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Abstract

The project consists of designing a pulse monitor that displays the high time, low time, duty cycle and frequency of a pulse train on an LCD.
The TTL compatible signal is inputted on P1.6 in a frequency range spanning 10Hz to 5,000Hz.

This project is implemented using the PCA architecture of the Atmel AT89c51RD2.

Components:

(1) HD44780U HITACHI Dot Matrix Liquid Crystal Display

(1) 8-bit flash microcontroller ATMEL AT89C51RD2

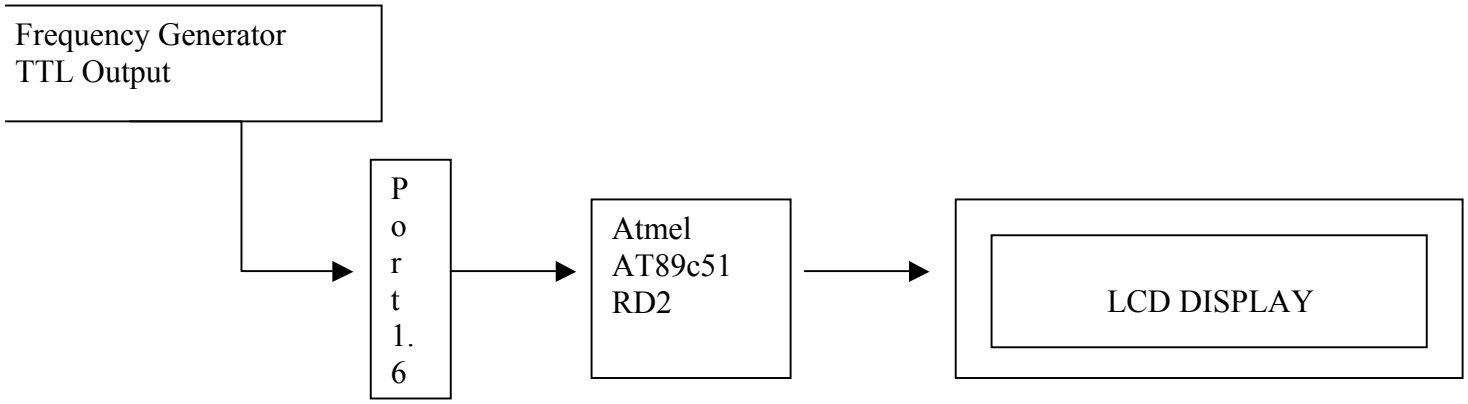


Figure 1: Connection Diagram

Description:

The project uses an interrupt routine that measures the time between falling edge to falling edge and rising edge to falling edge of pulses input on P1.6. The period and the high time are calculated in the interrupt routine. External variables pulse_high_time and period are global variables known to the main code. Next, the pulse period, high time, frequency and duty cycle are sent to each of the 4 lines of the LCD display.

Source Code Documentation:

The software makes use of 1 module

- **Interrupt routine design:**

1 – If the PCA overflow flag CF (in the CCON SFR) is set 1 when the PCA timer overflows.
    1.1 – Reset the flag CF
    1.2- Increment the PCA overflow variable

2- Otherwise must be a capture
    2.1 – Get the current read with CCAP3
    2.2- If rising edge
        2.2.1- set rising edge time to the current read
        2.2.2- set the rising edge overflow to the PCA overflow
    2.3- Otherwise if falling edge
        2.3.1- Measure the period using the current read and the last read
        2.3.2- Measure the high time using the current read and the rising edge time
        2.3.3- Set the current read to become the last read
        2.3.4- Reset the PCA overflow variable
        2.3.5- Reset the rising edge overflow variable

- **Initialize routine design**

1- Initialize the display
2- Initialize the PCA
    2.1- Put PCA in osc divide by 6 mode and enable PCA interrupt for overflow counting
    2.2- Put module 3 in rising and falling edge capture mode and enable interrupt
    2.3- Enable PCA clock source (PCA starts counting)
    2.4- Interrupt Enable Control 0

- **Main program design**

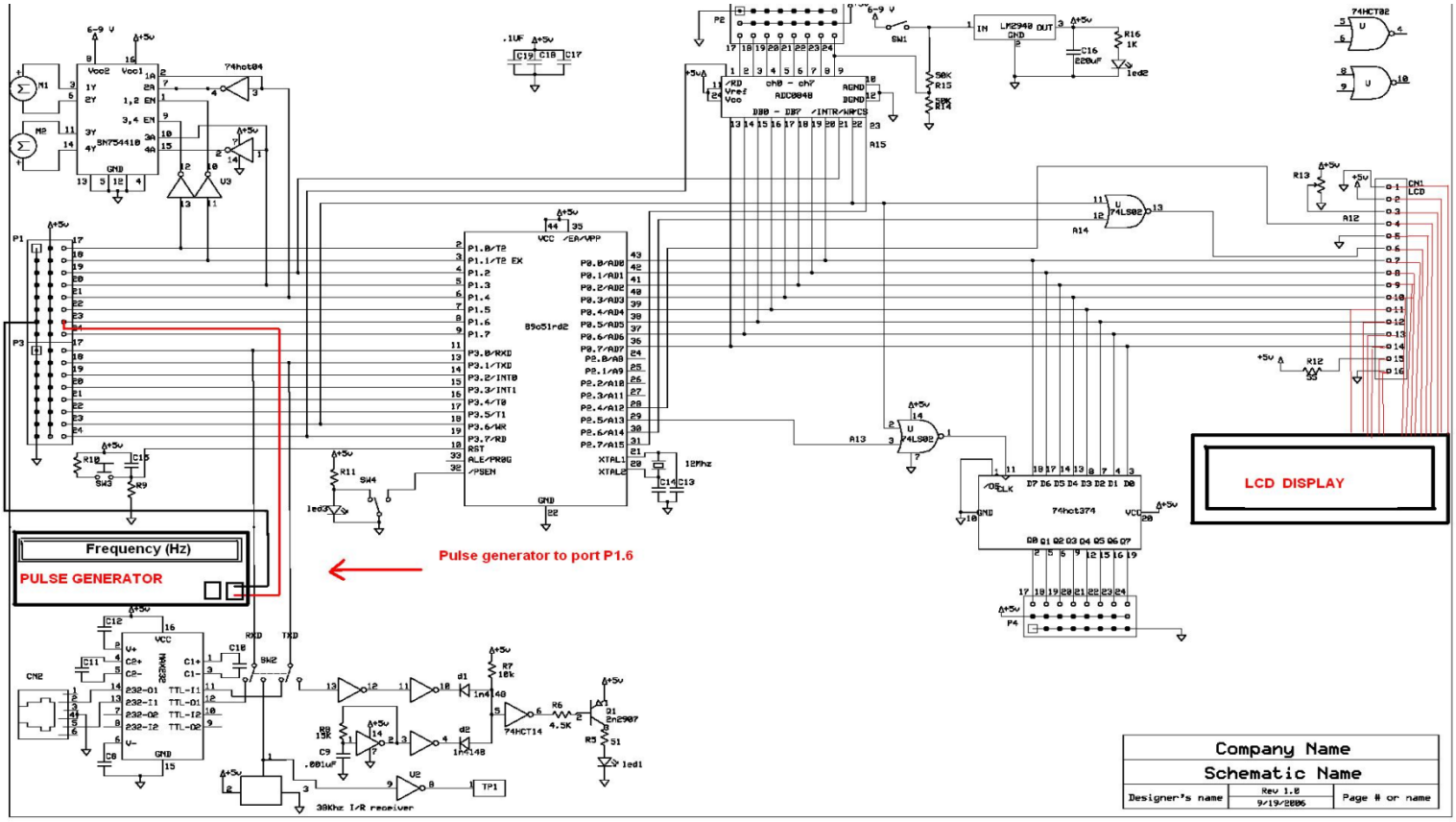
1- Call the Initialize() routine
2 – While loop
    2.1- Display pulse period
    2.2- Display the pulse high time

2.3- Display the pulse frequency
2.4- Display the pulse duty cycle

- **Display routine design**

1- LCD Delay module
2- LCD Driver module
3- Display text module
4- Display number module

Hardware design:



Schematic

The TTL output of the pulse generator has been connected to the port P1.6

Extra features

- Extended range of frequency measurements: 9.5 kHz

Conclusion

The device has been tested successfully and operates to reach a frequency of 9.5 kHz